2D and 3D Heterogeneous Photonic Integrated Circuits

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Abstract: This paper reviews 2D and 3D photonic integrated circuits and their applications in computing, networking, and signal processing. Various novel fabrication techniques leading to realization of chip-scale microsystems, and future prospects will also be discussed.

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1. Introduction
Exponentially increasing demands on data processing and communication are imposing serious challenges on future computing, networking, imaging, and sensing systems. Future information systems and cyberinfrastructures will inevitably employ more functional and energy-efficient microsystems integrated with heterogeneous technologies in a scalable and cost-effective manner. For electronics, it was more than four decades ago when Moore’s Law originally discussed [1] that the number of transistors which could be placed inexpensively on an electronic integrated circuit (EIC) doubled approximately every two years. As the number of transistors now exceed 10 billion per die, high-density integration naturally evolved from 2D to 3D integration by using through-silicon-vias (TSVs) or interposers. Heterogeneity in functionalities between variety of integrated modules help resource-efficient division of workload and task assignments across the system. Heterogeneous computing and processing units have been widely investigated for future computing systems. Similarly for photonics, increasing data processing demands and rapid advances in 2D photonic integrated circuits (PICs) have also led us to exponential increases in the number of devices integrated on a photonic die to coin a term ‘photonic Moore’s Law [2],’ and heterogeneous integration has been an important direction to incorporate diverse functionalities on a chip. For instance, silicon photonics achieves high-density, uniform, and repeatable integration of photonic components compared to other integration technologies, but requires III-V or other materials to be integrated together to incorporate energy-efficient lasers, electro-optical modulators, and other components. More recently, 3D photonic integration has emerged as very important steps to bring new functionalities and higher degrees of integration to microsystems. For instance, space division multiplexing (SDM) based on 3D photonic integration overcomes limitations imposed by 2D photonics in handling the spatial degree of freedom and polarization dependence resulting from the fact that all waveguides must lie within the same plane in 2D photonics. This paper discusses state-of-the-art heterogeneous 2D and 3D heterogeneous photonic integration technologies.

2. Motivation and Challenges for Heterogeneous Photonic Integration

Table 1. Various photonic integration platforms

<table>
<thead>
<tr>
<th>PIC Technology</th>
<th>Silicon PIC</th>
<th>GaAs PIC</th>
<th>InP PIC</th>
<th>Silica PIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leveraging Technologies</td>
<td>Leverages Silicon CMOS industry</td>
<td>Leverages GaAs HBT industry</td>
<td>Leverages InP HBT industry</td>
<td>No electronics industry</td>
</tr>
<tr>
<td>Photonic-Electronic Integration</td>
<td>“Silicon CMOS photonics”</td>
<td>“GaAs OEIC”</td>
<td>“InP OEIC”</td>
<td>No electronics industry</td>
</tr>
<tr>
<td>Waveguide Confinement</td>
<td>Strong confinement, Si/SiO₂</td>
<td>Medium confinement, GaAs/AlGaAs</td>
<td>Medium confinement, InP/InGaAsP</td>
<td>Weak confinement, GeO₂, etc doping</td>
</tr>
<tr>
<td>Typical MFD</td>
<td>&lt; 0.5 micron Confinement</td>
<td>&gt; 2 micron Confinement</td>
<td>&gt; 2 micron Confinement</td>
<td>&gt; 5 micron Confinement</td>
</tr>
<tr>
<td>Optical Gain and Optical Modulation</td>
<td>No gain, no Pockel's effect</td>
<td>Efficient gain, strong Pockel's effect</td>
<td>Efficient gain, strong Pockel's effect</td>
<td>No gain, no Pockel's effect</td>
</tr>
<tr>
<td>Wafer Size</td>
<td>≥300 mm wafers</td>
<td>≥200 mm wafers</td>
<td>≥100 mm wafers</td>
<td>≥200 mm wafers</td>
</tr>
</tbody>
</table>

Primary motivation for photonic integration can be to reduce cost, power consumption, size, packaging complexity, and failures (FIT) and to enhance performance. On the other hand, challenges in photonic integration are to achieve high yield, to realize process compatibility, to overcome power/thermal density limitations, and to reduce thermal/signal crosstalk. As Table 1 summarizes, there are various photonic integration platforms with advantages and disadvantages. Heterogeneous photonic integration provides an opportunity for combining advantages from multiple photonic integration platforms. For instance heterogeneous integration of silicon, InP, and silica photonic integration...
platforms can combine gain and Pockel’s effects available in III-V materials, low-loss waveguides available in silica and silicon nitride materials, and compact waveguides available on silicon wafers. Monolithic Integration includes hetero-epitaxy of group III-V on group IV, hetero-epitaxy of group IV on group IV, and amorphous deposition followed by rapid melt growth, etc. Hybrid integration includes flip-chip bonding and wafer bonding. Wafer bonding techniques include hydrophobic wafer bonding, and hydrophilic wafer bonding. While achieving monolithic integration of heterogeneous material platforms by hetero-epitaxy and rapid melt growth can ideally achieve intimate mechanical, thermal, optical, and electrical binding between the heterogeneous platforms, there are significant challenges in achieving hetero-epitaxy overcoming lattice mismatch with low defect densities or rapid melt growth at reasonable temperature levels. On the other hand, hybrid integration of heterogeneous material platforms by utilizing wafer bonding, flip-chip bonding, etc., can prove to be a very practical approach. Motivation for 3D heterogeneous integration is to extend the benefit of 2D heterogeneous integration to 3D and to achieve higher density integration than 2D. On the other hand, the challenges for 3D integration far exceeds those of 2D integration. The following discusses 3D photonic integration.

3. 3D Photonic Integration Techniques

Figure 1. (a) Schematic illustration of 3D photonic inscribing method where optical pulse energy, pulse repetition rate, and waveguide scan speed are adjusted to optimize the quality of the inscribed waveguide, (b) photograph of the sample on a translation stage scanning in x-y-z directions under the focused femtosecond-laser illumination, (c) schematic of the laser pulses in the material, (d-e) photographs of a single ring 3D waveguide fan-out device composed of directly laser writing butt coupled to a 2D waveguide block for orbital angular momentum applications [3, 4]; (f) 3D CAD design of the multi-ring 3D waveguides and (g) photograph of the multi-layer silicon nitride waveguides interfacing with (h) the multi-ring (64 aperture) 3D waveguides, (i) 3D CAD design of 16x16 waveguides, and (j) photographs of the 16x16 rectangular lattice. Another method of 3D integration by stacking illustrated in Figure 2 shows (a) future 3D electronic-photonic integrated circuit processor extending the electronic 3D IC by adding a silicon photonic interconnection plane and (b) fabricated silicon photonic interconnection switch [5].
Figure 3 shows (a) a conceptual schematic of a photonic lantern, (b) a 3D CAD design, and (c-d) the mode pattern and a photograph of the fabricated 3D waveguide. (g) Stacking of multiple 2D layers (e.g., five layers) for arbitrary waveform shaping, (h) fabricated three layer silicon nitride/silicon dioxide OAM device.

Figure 2. (left) Future 3D electronic-photonic integrated circuit processor consisting of silicon photonic interconnect plane, memory plane, and processor plane together with an external optical frequency comb source, (right) silicon photonic interconnection switch [5].

Figure 3. (a) Schematic and (b) 3D CAD of the photonic lantern devices. (c-d) mode pattern and photograph of the fabricated 3D waveguide [7]. (e-f) schematic of 2 layer and 3 layer coupling waveguides. (g) Stacking of multiple 2D layers (e.g., five layers) for arbitrary waveform shaping, (h) fabricated three layer silicon nitride/silicon dioxide OAM device.

4. Summary

3D photonic integration emerges as a powerful new dimension to the current photonic integration platform. Laser inscribing provides a free-form method to create arbitrary shape embedded waveguides in 3D and also offers a method to achieve photonic wirebonding. Multilayer stacking facilitates creation of 3D photonic integrated circuits by using conventional lithography and deposition methods. 2D/3D heterogeneous photonic integration is essential for future microsystems aiming at scalability, high-performance, and cost effectiveness.

References


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