Advanced Modulation for Datacenter Interconnect

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Abstract: We present DSP enabled advanced modulation techniques for 100G per lambda data center optical modules based on low cost and power efficient directly modulated laser transmitters and single photodiode direct detection receivers.

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1. Introduction

The recent adoption of PAM4 optical modulation, alongside with Reed-Solomon FEC, by the IEEE 400 Gb/s Ethernet Task Force heralds a new era for client optics [1]. The trend is clear: advanced modulation, digital signal processing, and coding will play an increasingly important role in the design of future datacenter networks. In some ways, this trend mirrors and benefits from the developments in metro and long haul fiber optic systems. However, the datacenter presents very different engineering tradeoffs, requiring unique solutions [2]. For example, datacenter applications typically require a physical layer with a relatively low latency of ~ 100 ns or less; this can pose a significant constraint on FEC and DSP designs. Datacenter switch fabrics scale better with high radix or a large number of high speed ports, which drives the continuous evolution toward lower power and smaller form factor optical modules. Finally, the massive deployment of fiber optic links in mega datacenters can only be achieved with low cost. All of these factors are expected to influence the development of advanced modulation techniques for datacenter interconnects.

The design of datacenter modules is further complicated by the myriad of technologies that play in this space. For example, one may contemplate TOSA designs based on VCSEL, DML/DFB, EML, and MZM transmitters, InP and SiP material platforms, single channel versus N channel parallel or WDM systems, SMF, MMF, multicore or other novel fibers. In such a scenario, with so many design choices and associated complex engineering tradeoffs, one may consider archetype datacenter system architectures as a guide. Here we propose an archetype system design shown in Fig. 1, based on the concept of the simplest optics possible: a DML transmitter and single PD receiver [3].

Fig. 1: An archetype 100 GbE per lambda system architecture based on DML and DSP at Tx and Rx.
The inset of Fig. 1 shows a measured optical eye diagram for a 52 Gb/s PAM4 DML transmitter with a bandwidth of ~22 GHz. PAM4 modulation, combined with FEC and modest receiver equalization, provides a straightforward path to scale datacenter networks to 50 Gb/s per lane using existing 25G DML technology. It would be very desirable to leverage the significant industry investments made in developing high speed DMLs for even higher capacity. This begs the question: is there anything left in a DML beyond 50 Gb/s? We can estimate the Shannon capacity for the DML channel from the received SNR. The inset of Fig. 1 shows a measured electrical SNR as a function of frequency at the receiver using a digital discrete multitone (DMT) technique at an average optical power of -2 dBm. Summing the sub-channel Shannon capacities $\delta C = \delta f \log_2 (1+SNR)$ over all frequency bins $\delta f$, we obtain a total capacity $C = 179$ Gb/s for this channel. Thus, there is ample room to continue scaling the DML to 100 Gb/s, and perhaps even beyond, by using advanced modulation and coding. In the proposed architecture of Fig. 1, the higher complexity required for scaling bitrate per lambda to 100 Gb/s is placed in the DSP function at the transmitter and receiver; for example, the inset of Fig. 1 shows the DSP block diagram for a novel DFT-S PAM4 modulation discussed below. This archetype system concept assumes complex CMOS ASICs scale better in cost at high volumes compared with complex or ultra-high speed electro-optics. In the sequel, we review our research on DSP enabled advanced modulation formats for achieving future 100 GbE per lambda optical client modules.

2. Comparison of Modulation Formats

Figure 2 shows the results of a Monte-Carlo simulation analysis, comparing several interesting 100G modulation formats, including Nyquist PAM4, PAM4 with partial response (PR) equalization (PAM4 PR FFE), and DMT [4-6]. PAM4 and DMT are perhaps the two most studied advanced modulation formats for 100G per lambda. In addition, we show results for several novel DSP based modulation techniques, which we call DFT-S QAM and DFT-S PAM, based on a version of the DFT spread technique [7]. The table in Fig. 2 describes the system parameters of the simulations. All modulation formats considered, except PAM4 PR FFE, assume a DSP/DAC at transmitter and ADC/DSP at receiver. While a high resolution DAC and ADC enable powerful DSP based equalization in the Tx and Rx, the CMOS DAC/ADC analog bandwidth is currently limited to ~20 GHz. The PAM4 PR FFE system requires only a 2-bit DAC for generating PAM4 modulation; hence a wider 30 GHz transmitter analog electrical bandwidth is assumed in this case. As indicated in the table of simulation parameters, linear equalization, 31-tap time domain T/2 FFE or 1024 point FFT with 1-tap frequency domain equalization, is employed at the receiver to compensate for the limited TOSA bandwidth, and fiber dispersion. The total simulated bit rate is 106 Gb/s, including 3% overhead for a low-latency IEEE standard KP4 FEC with BER threshold at $3 \times 10^{-4}$.

![Graph](image_url)

**Fig. 2:** Monte-Carlo simulation results for a). B2B, b). 10 ps/nm, c). RIN power penalty; d). system simulation parameters.
The simulation results reveal some interesting trends. DMT suffers a significant power penalty due to its high peak-to-average power ratio (PAPR). The DFT-S techniques improve the PAPR by concentrating signal power in a single carrier in the 0 to 20GHz frequency band where SNR is relatively flat, and using the rest of signal power to squeeze out the maximum capacity from the remaining channel bandwidth. The PAM4 analog Tx with wider 30 GHz bandwidth also benefits from a lower PAPR, and the partial response equalization at Rx induces less noise enhancement compared with PAM4 full response. However, we note that clock recovery (not included in the simulations) may be more challenging for partial response systems. Figure 2 also shows the RIN power penalty for each modulation format. We observe a higher RIN penalty for less efficient modulation techniques which require higher receiver optical power, and suffer higher ISI penalties. DMLs for 100G per lambda applications must meet stringent laser RIN specifications of -142 dB/Hz to -145 dB/Hz, depending on the choice of modulation.

3. Experiments

Figure 3 shows our experimental setup for 112 Gb/s per lambda DML system [7]. In this experiment, the DAC analog bandwidth was limited to < 20 GHz, and hence only digitally synthesized modulation formats are tested, with digital pre-equalization employed to mitigate limited Tx analog bandwidth. The DML is the same device which generated the 50G PAM4 eye diagram shown in Fig. 1. BER is measured offline using Matlab signal processing very similar to the simulations in Fig. 2. The experimental results confirm a superior performance of DFT-S PAM (labeled as O-PAM-DMT in the plot) compared with DMT and Nyquist PAM. Note due to the interaction of laser chirp and chromatic dispersion in this experiment, the effective channel bandwidth was enhanced at 1310nm by adding 12 km of SMF; this particularly benefits the Nyquist PAM modulation by reducing the noise enhancement in linear equalization. Good experimental results at 112 Gb/s per lambda have also been reported recently for PAM4 modulation with a partial response MLSE receiver [6]. This experimental data, as well as research by other groups, demonstrates feasibility of 100G per lambda DML systems based on advanced modulation techniques and DSP.

4. References


